WHAT IS CLAIMED:

1. A system for simulating an electronic circuit model that has been coded into a hardware description language (HDL), comprising:

a processor having memory for storing a program that is capable of being executed by said processor said program directing the operation of said processor to:

convert the HDL coded electronic circuit model to binary object code; and

simulate the electronic circuit by utilizing said binary object code.

2. The system of claim 1, wherein said program directs said processor to convert the HDL coded electronic circuit model to binary object code by directing said processor to translate the HDL coded electronic circuit model into an intermediate program language code and to compile said intermediate program language code to said binary object code.

3. The system of claim 2, wherein said intermediate program language code is a C program language code.

4. The system of claim 3, wherein said C program language code is grouped into code types selected from a group consisting of: evaluation C code and scheduling C code.

5. The system of claim 1, wherein said binary object code performs operations that are selected from a group consisting of: initial/always block operations, timing-free procedural

operations, task procedural operations, function procedural operations, event control operations, delay control operations, scheduled procedural operations, declarative gate operations, continuous assignment operations, user-defined primitive operations, implicit wired operations, delay path operations, system task operations, and system service operations.

6. The system of claim 1, wherein said program directs said processor to simulate the electronic circuit by utilizing said object code to make calls to a programming language interface (PLI).

7. The system of claim 1, wherein said binary object code is utilizable by substantially all types of simulators.

8. A method for simulating an electronic circuit model that has been coded into a hardware description language (HDL), comprising:

reading the HDL coded electronic circuit model;

converting the HDL coded electronic circuit model into a linkable simulation program; and

simulating the operation of the electronic circuit by utilizing said linkable simulation program.

9. The method of claim 8, wherein said step of converting comprises the steps of translating the HDL coded electronic circuit model into an intermediate program language code and compiling the intermediate program language code to said linkable simulation program.

10. The method of claim 9, wherein said intermediate program language code is a C program language code.

11. The method of claim 10, wherein said step of converting further comprises the step of group said C program language code into types selected from a group consisting of: evaluation C code and scheduling C code.

12. The method of claim 8, wherein said linkable simulation program performs operations that are selected from a group consisting of: initial/always block operations, timing-free procedural operations, task procedural operations, function procedural operations, event control operations, delay control operations, scheduled procedural operations, declarative gate operations, continuous assignment operations, user-defined primitive operations, implicit wired operations, delay path operations, system task operations, and system service operations.

13. The method of claim 8, wherein said step of simulating comprises making calls to a programming language interface (PLI).

14. The method of claim 8, wherein said linkable simulation program is utilizable by substantially all types of simulators.

15. A system for simulating an electronic circuit model that has been coded into a hardware description language (HDL), comprising:

processing means for executing a program, wherein said program includes a conversion means for converting the HDL coded electronic circuit model into a simulator-operable program and a simulation means for simulating the HDL coded circuit model by utilizing said simulator-operable program to make calls to a programming language interface (PLI).

16. The system of clam 15, wherein said simulator-operable program comprises binary object code.

17. The system of claim 15, wherein said conversion means includes means for translating the HDL coded electronic circuit model into an intermediate program language code and means for compiling said intermediate program language code to said simulator-operable program.

18. The system of claim 17, wherein said intermediate program language code is a C program language code.

19. The system of claim 18, wherein said C program language code is grouped into code types selected from a group consisting of: evaluation C code and scheduling C code.

20. The system of claim 15, wherein said simulator-operable program performs operations that are selected from a group consisting of: initial/always block operations, timing-free procedural operations, task procedural operations, function procedural operations, event control operations, delay control operations, scheduled procedural operations, declarative gate operations, continuous assignment operations, user-defined primitive operations, implicit wired operations, delay path operations, system task operations, and system service operations.

21. The system of claim 15, wherein said simulator-operable program is utilizable by substantially all types of simulators.